Centipede Wiring Diagram (037432-01 C)

Regulator/Audio II PCB

The Regulator/Audio II PCB has the +5 VDC logic power to controlling the audio from the game PCB.

Regulator Circuit

The regulator consists of voltage pass transistor Q3 and Q25 driver to the circuit to accurately regulates the logic power to +5 VDC. The voltage from the +5 VDC and ground inputs to the regulator eliminates a reduced voltage due to the harness between the regulator and the resistor R6. Once adjusted, the voltage at the input is constant at +5 VDC.

Regulator Adjustment

1. Connect a voltmeter between +5 VDC and ground of the game PCB.
2. Adjust variable resistor R8 on the game PCB for +5 VDC reading on the voltmeter.
3. Connect a voltmeter between the Regulator/Audio II PCB and +5 VDC of both harness connectors on both the game PCB and Audio II PCB.
4. Adjust R8 until -5 VDC reading is obtained.

Audio Circuit

The audio circuit consists of two in-series transformers. Each transformer consists of a T20, with an effective gain of 22.
American-Made Coin Door Schematic (036835-01 B)

British-Made Coin Door Schematic (037050-01 A)

Denotes a test point
Synchronizer

CAT Box Preliminary Set-up
1. Remove:
   - The electrical power from the game.
   - The wiring harness from the game PCB.
   - The game PCB from the cabinet.
   - The MPU chip C2 from the game PCB.
2. Connect:
   - The extender cables to the game PCB and the wiring harness.
   - The test points A0 and A2 on the game PCB.
   - The CAT Box flex cable to the game PCB test edge connector.

Diagnostic Tests

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Use of Test</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Hold the main switch closed while setting the off/next switch to the on position.</td>
<td>The monitor displays the color hue adjustment pattern of 16 rectangles, as shown. Do not attempt any color hue or brightness adjustments unless you are a qualified color TV technician. Pass Yellow/Green, Orange, White, Yellow/Red, Deep Blue, Red, Navy Blue, Blue, Dark Blue.</td>
</tr>
<tr>
<td>2. Activate any of the coin switches on the coin door.</td>
<td>A convergence pattern appears with a grid of white dots on a black screen. Do not attempt any convergence adjustments unless you are a qualified color TV technician.</td>
</tr>
<tr>
<td>3. Set the test switch to the off position.</td>
<td>Check all mode display and adjust brightness if necessary.</td>
</tr>
</tbody>
</table>

ATARI
Centipede™

Synchronizer
CAT Box Preliminary Set-Up
Power Input
Microprocessor
Address Decoder
RAM
ROM
Memory Map

Section of 037241-01
© 1981 Atari, Inc.

Testing the RAM
1. Perform the CAT Box Preliminary Set-Up.
2. Set the CAT Box switch to:
   - TESTER mode.
   - DBUS SOURCE 15V.
   - BYTES to 1024.
   - R/W MODE to 0/1.
   - Key in 0000.
   - Set R/W MODE to 0.
   - Set R/W MODE to 1.
3. If the CAT Box reads "RAM ERROR LED 9" shows the failing side, PLAY switch is enabled.
4. If the comparators end...
RAM
Box preliminary set-up.
switches as follows:
RESET TO ADDR
4 (OFF)
Q to PULSE, then to OFF.

To Sheet 2, Side B

Denotes a test point

Denotes a test point

Memory Map

<table>
<thead>
<tr>
<th>HEXA ADDRESS</th>
<th>READ</th>
<th>WRITE</th>
<th>DATA</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000-0FFF</td>
<td>D</td>
<td>D</td>
<td>D</td>
<td>PAYLOAD RAM</td>
</tr>
<tr>
<td>00H-07H</td>
<td>D</td>
<td>D</td>
<td>D</td>
<td>Motion Object Picture</td>
</tr>
<tr>
<td>08H-0FH</td>
<td>D</td>
<td>D</td>
<td>D</td>
<td>Motion Object Vert.</td>
</tr>
<tr>
<td>10H-11H</td>
<td>D</td>
<td>D</td>
<td>D</td>
<td>Motion Object Horiz.</td>
</tr>
<tr>
<td>12H-17H</td>
<td>D</td>
<td>D</td>
<td>D</td>
<td>Motion Object Color</td>
</tr>
</tbody>
</table>

Option Switch 1 (E-a On)
Option Switch 2 (E-b On)

Horizontal Mini-Trak Ball™ Inputs
VISLINK (1 = Vislink)
Cocktail Cabinet (1 = Cocktail)
R.C.L. Coin Switches (5 = On)

Player 2 Fire Switch (6 = On)
Player 1 Fire Switch (6 = On)
Player 1 Start Switch (6 = On)
Player 1 Start Switch (6 = On)
Player 2 Start Switch (6 = On)

Player 1 Joystick P.L. Down, Up
Player 2 Joystick (E-a On)

Custom Audio Chip

PayLoad Color RAM
Motion Object Color RAM

EA ROM Address & Data Latch
EA ROM Control Latch
EA ROM Read Data

IRQ Acknowledge

Left Coin Counter (1 = On)
Center Coin Counter (1 = On)
Right Coin Counter (1 = On)
Player 1 Start LED (6 = On)
Player 2 Start LED (6 = On)
Test Ball™ Flip Control (6 = Player 1)

WATCHDOG
Clear Mini Trak Ball™ Counters

Program ROM
Centipede Playfield RAM
Testing the Playfield RAM

1. Perform the CAT Box preliminary set-up.
2. Set the CAT Box switches as follows:
   a. Press TESTER RESET
   b. DBUS SOURCE TO ADDR
   c. BYTES to 64K
   d. R/W MODE to (OFF)
   e. R/W to WRITE
   f. KEY to 040
   g. Set R/W MODE to PULSE, then to (OFF)
   h. R/W to READ
   i. Set R/W MODE to PULSE, then to (OFF)

3. If the CAT Box reads an address that doesn't compar, the COM-
   PARE ERROR LED lights, the ADDRESS/SIGNATURE display
   shows the failing address location, and the ERROR DATA DIS-
   PLAY switch is enabled.

4. If the COMPARnej ERROR LED does not light, re-try 0400 and re-
   peat the test with the DBUS SOURCE switch set to ADDR. This
   ensures that the data bits at address 0400 will go high. If the
   COMPARnej ERROR LED does not light after this step, the Play-
   field RAM is good.

Playfield Address Selector
The Playfield Address Selector controls the access to the playfield memory.
It allows either the game MPU or the sync generator to scan the playfield mem-
ory. The Playfield Address Selector consists of multiplexers A5, and P7 and
P8 is controlled.

When E7 on pin 1 of P5 and P7 is low and pin 15 on P7 is low, the Playfield
Address Selector receives B1, 16H, 32H, and 64H on P5 and 16H, 32H, 64H, and
128H on P7 from the sync generator. These signals enable the sync generator
circuits to access the playfield memory.

When 45 goes high the game MPU addresses the playfield memory via
A15-4A8 for the positioning of the graphics. During horizontal blanking (pin 15
of P7 is high) the outputs of P7 (PFAA, PFA7) are held high enabling the motion
circuitry to access the playfield memory for the motion objects to be
displayed.

Motion Object Circuitry (Vertical)
The Motion Object Circuitry (vertical) receives playfield data and verti-
ical sync generator circuits to generate the vertical component of the motion
of the playfield memory and 1V-12V from the sync generator are con-
trolled. The output is gated by A7 when a motion object is on one of the sixteen
lines selected by B6 and gate B7. A low on D7 pin 6 indicates the presence of
one of the vertical lines during non-active video time. This signal (MATCH-
fiers in the picture data circuitry.

When 256H on pin 1 of D7 goes high, 1V, 2V, 4V and PCD are selected. In
the latched output of E6 is selected. The output of D7 is EXCLUSIVE OR
sent to the picture data selector circuitry as motion graphic address (MDA)
input to EXCLUSIVE OR gate E7 is PCD from the playfield code multi-
plier when high causes the output of E7 to be complimented. For example, if M
PCD causes MGA0/MGA3 to go high. This causes the motion object to
top to bottom.
Testing the Option Switches

1. Perform the CAT Box preliminary set-up.
2. Set the CAT Box switches as follows:
   a. DBUS SOURCE to DATA
   b. BYTES to 1
   c. RW to READ
   d. Key in address 0000 (N6) or 0011 (N8)
   e. RW MODE to STATIC
3. Activate the switch while monitoring the DATA DISPLAY. The DATA DISPLAY will change if the switch is operating properly.

Coin Counter Output Circuit

This circuit consists of coin counter drivers Q6, Q7, and Q8 and data latch M70. The circuit is addressed by the MPU on A8-A30 and written by the MPU on data line DB7. When the input to a driver is clocked high, its collector goes low grounding the return of the coin counter in the coin door.

Mini-Trak Ball™ Circuitry

Testing the Mini-Trak Ball™ Inputs

1. Perform the CAT Box Preliminary Set-up.
2. Set the CAT Box switches as follows:
   a. DBUS SOURCE to DATA
   b. BYTES to 1
   c. RW to READ
   d. Key in address 0000 (vertical) or 0001 (horizontal)
   e. RW MODE to PULSE
3. Spin the Mini-Trak Ball™ while monitoring the DATA DISPLAY. The DATA DISPLAY will change if the Mini-Trak Ball input is operating properly.
Testing the Player Inputs

1. Perform the CAT Box Preliminary Set-up.
2. Set the CAT Box switches as follows:
   a. DBUS SOURCE to DATA
   b. BYTES to 1
   c. RW to READ
   d. Key in address (0000) (self-check switch only) 0001 (all others)
   e. RW MODE to DATAC
3. Activate the following player input switches, one at a time, while monitoring the DATA DISPLAY:
   a. Coin Right
   b. Coin Left
   c. SLAM
   d. FIRE
   e. START 1
   f. START 2
4. The DATA DISPLAY will change if the switches are operating properly.

Audio Output Circuity

1. Perform the CAT box preliminary set-up.
2. Set the CAT Box switches as follows:
   a. DBUS SOURCE to DATA
   b. BYTES to 1
   c. RW to WRITE
   d. Key in address or press ADDRESS INC
   e. Press DATA SET
   f. Key in data
   g. Set RW MODE to PULSE, then to OFF.
   h. For each address, repeat sequence starting at Step 1.

<table>
<thead>
<tr>
<th>ADDRESS DATA</th>
<th>RESULTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>100F 00</td>
<td></td>
</tr>
<tr>
<td>100F 00</td>
<td></td>
</tr>
<tr>
<td>1000 55</td>
<td></td>
</tr>
<tr>
<td>1001 AP</td>
<td>Pure tone is heard from channel 1 output.</td>
</tr>
<tr>
<td>1001 00</td>
<td>Channel 1 output is turned off.</td>
</tr>
<tr>
<td>1002 AP</td>
<td>Pure tone is heard from channel 2 output.</td>
</tr>
<tr>
<td>1003 00</td>
<td>Channel 2 output is turned off.</td>
</tr>
<tr>
<td>1004 55</td>
<td></td>
</tr>
<tr>
<td>1005 AP</td>
<td>Pure tone is heard from channel 3 output.</td>
</tr>
<tr>
<td>1006 00</td>
<td>Channel 3 output is turned off.</td>
</tr>
<tr>
<td>1006 55</td>
<td></td>
</tr>
<tr>
<td>1007 AP</td>
<td>Pure tone is heard from channel 4 output.</td>
</tr>
<tr>
<td>1007 00</td>
<td>Channel 4 output is turned off.</td>
</tr>
</tbody>
</table>

Denotes a test point

Video Output Circuitry

The video output circuit receives motion object, playground, address and data inputs and produces a video output to be displayed on the game monitor. In order to read out of the color RAM, GRY0 and GRY1 from the motion object circuitry are multiplied with AREA0 and AREA1 from the playground circuit by E8. The output, selected by GRY0 or GRY1, is RAMA0-RAM3 (RAM ADDRESS).

RAMA0-RAM3 are applied to color RAM DB. The colors red, green, blue and an alternate color bit are outputs. The three color bits are latched by A8 as the game video in the three basic colors (or shades of gray in a black and white monitor). When the alternate color bit DB1 (pin 11) is active, an alternate shade of blue or green is available.

The following conditions, along with the various combinations of COLOR 1 (red), COLOR 2 (green) and COLOR 3 (blue), provide 6 extra colors for a total of 14.

1. If A8 pin 11 is low, transistor Q5 conducts and draws current from COLOR 1 and COLOR 2 are off.
2. If A8 pin 10 is low, transistor Q4 conducts and draws current from COLOR 1 and COLOR 2 are off.

High Score Memory Circuitry

The High Score Memory circuit stores the three best scores and other pertinent information. These scores are saved even if power is removed from the game. The High Score Memory circuit consists of an erasable programmable ROM, E5, latches E4, H4, J4, buffer H5 and timer A11.

A7 produces a 0.15V square wave at a 1V rate. This signal, when a 5V forward biased diode CAD and allows capacitor CAD to charge to +3V. When the signal is low, CAD is cut off and CM4 is forward biased which causes CM4 to develop a charge. CM4 charges to approximately +3V. This is the potential required for EROM 20 to operate.

The MPU addresses the EROM (A01-ABS) when the A8DI0 gates WRITE2 at gate A4. The trailing edge of the gated pulse latches the address information to the EROM E5 via J4. Data is latched by H4 at the same time. The EROM mode (read, write or erase) is determined by the A00-001 latch E4. A low A00-001 gates WRITE2 at gate A4. A trailing edge of this gated pulse latches the data into the EROM E5 via latch H4.

Data is read from the EROM when EREAD on pin 1 of buffer H4 goes low.